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(54) METHOD FOR ETCHING SILICON WAFER AND METHOD FOR DIFFERENTIATING FRONT AND REAR SURFACE OF SILICON WAFER USING THE SAME

(57)Abstract:
PROBLEM TO BE SOLVED: To provide an etching method of a silicon wafer, by which excellent mirror finish flatness can be obtained on the front surface and the rear surface is a little rough.
SOLUTION: This is to provide an improved version of a silicon wafer etching method in which an acid etchant and an alkaline etchant are individually stored in a plurality of tanks, and a silicon wafer having a process modified layer formed through a lapping process and a subsequent cleaning process is sequentially immersed in the acid etchant and the alkaline etchant. In this method, the alkaline etching is treated after the acid etching, the concentration of the alkaline etchant is set to be 8 mol/l or more, and the etching rate of the acid etching is set to be 0.2 μm/sec or more in total in the front and rear surfaces of the silicon wafer.

* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1]Acid etching liquid and alkali etching liquid are stored in two or more etching tubs, respectively, In an etching method of a silicon wafer which immerses a silicon wafer which has the damaged layer which passed through a washing process following a lapping process one by one in acid etching liquid and alkali etching liquid, Alkali etching makes concentration of a line crack and said alkali etching liquid 8 or more mol/l after acid etching, And an etching method of a silicon wafer making an etching rate of acid etching into a second in 0.2micrometers /or more in the sum total with which the surface and a rear face of said silicon wafer were doubled.
[Claim 2]The etching method according to claim 1 which sets a sum total machining allowance of an acid etching tub to 13-25 micrometers in the sum total with which the surface and a rear face of a silicon wafer were doubled, and sets a sum total machining allowance of an alkali etching tub to 5-13 micrometers in the sum total with which the surface and a rear face of a silicon wafer were doubled.
[Claim 3]The etching method according to claim 1 or 2 which makes the number of acid etching tubs one to 3 tub for the number of etching tubs, and makes the number of alkali etching tubs one to 3 tub.
[Claim 4]Claims 1 thru/or 3 in which acid etching liquid contains fluoric acid and nitric acid, respectively are the etching methods of a statement either.
[Claim 5]The etching method according to claim 4 with which acid etching liquid contains further acetic acid, sulfuric acid, or at least one sort of phosphoric acid.
[Claim 6]Claims 1 thru/or 3 in which alkali etching liquid contains sodium hydroxide or a potassium hydrate are the etching methods of a statement either.
[Claim 7]How to carry out mirror polishing only of the surface of a silicon wafer etched by a method according to any one of claims 1 to 6, and differentiate a surface and rear surface of said wafer.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to an improvement of the method of carrying out etching removal of the damaged layer of the wafer surface to generate in the manufacturing process of a silicon wafer. It is related with the method of carrying out mirror polishing only of the surface of the etched wafer in detail, and differentiating a wafer surface and rear surface.
[0002]
[Description of the Prior Art]Generally the manufacturing process of a semiconductor silicon wafer, The wafer produced from the silicon single crystal ingot pulled up by starting and slicing is constituted from camfering, mechanical polishing (wrapping), etching, mirror polishing (polishing), and a process to wash, and it is produced as a wafer which has highly precise display flatness. Some of the processes are replaced by the purpose, or the multiple-times loop of these processes is carried out, or other processes, such as heat treatment and grinding, are added, they are replaced, and various processes are performed. The silicon wafer which passed through machining processes, such as block cutting, outer diameter grinding, a slicing, and wrapping, has the damaged layer, i.e., a damaged layer, on the surface. Since a damaged layer induces crystal defects, such as slipping dislocation, in a device fabrication process, reduces the mechanical strength of a wafer and has an adverse effect on an electrical property, it must be removed thoroughly.
[0003]An etching process is performed in order to remove this damaged layer. There are acid etching which uses acid etching liquid, such as mixed acid, and alkali etching using alkali etching liquid, such as NaOH, in an etching process. However, by performing acid etching, the display flatness obtained by wrapping is spoiled and the unevenness called the wave of mm order and a peel to the etching surface occurs. There was a problem of the pit (this is hereafter called facet.) whose sizes the local depth is a number - about 10 micrometers of numbers in several micrometers occurring by performing alkali etching.
[0004]As a method of solving the above-mentioned problem, acid etching is performed after alkali etching and the wafer processed by the processing method and this method of the wafer which makes the machining allowance of the alkali etching at this time larger than the machining allowance of acid etching is proposed (JP,11-233485,A). A damaged layer is removed with a described method, maintaining the display flatness after wrapping, flat-surface granularity is improved, and it becomes possible especially to produce the wafer which has the etching surface which has smooth uneven shape more shallowly, and where neither particle nor contamination generates a local facet easily. On the other hand, since detection of the wafer existence in the conveyance system of a device process was performed by the wafer rear face, detection difficulty and problems, such as carrying out wrong detection, had arisen that the wafer rear face which carried out mirror polishing of the surface was mirror finished surface form.
[0005]
[Problem(s) to be Solved by the Invention]With the wafer (henceforth PW;Polished Wafer) which carried out mirror polishing, the surface of the wafer shown in above-mentioned JP,11-233485,A. There was a problem which has the good display flatness for which a device maker asks, and cannot obtain a wafer with small rear-face granularity of PW.
[0006]In the wafer which carried out mirror polishing of the surface, the purpose of this invention is to provide the etching method of the silicon wafer which obtains good display flatness and in which rear-

face granularity becomes small. Another purpose of this invention is to provide the surface and rear surface differentiation method of the silicon wafer which has display flatness with highly precise wafer both sides, and small surface roughness, and makes the surface and rear surface of a wafer identifiable by viewing.

[0007]

[Means for Solving the Problem]An invention concerning claim 1 stores acid etching liquid and alkali etching liquid in two or more etching tubs, respectively, It is improvement of an etching method of a silicon wafer which immerses a silicon wafer which has the damaged layer which passed through a washing process following a lapping process one by one in acid etching liquid and alkali etching liquid. Alkali etching is performed after acid etching, and this characteristic composition makes concentration of alkali etching liquid 8 or more mol/l, and is in a place which makes an etching rate of acid etching a second in 0.2micrometers /or more in the sum total with which the surface and a rear face of a silicon wafer were doubled. In an invention concerning claim 1, alkali etching is performed after acid etching, A wafer by which specified concentration of alkali etching liquid and an etching rate of acid etching on the above-mentioned conditions, immersed a wafer in alkali and acid etching liquid one by one, and the etching process was carried out can make rear-face granularity small while maintaining display flatness obtained by a lapping process.

[0008]An invention concerning claim 7 is the method of carrying out mirror polishing only of the surface of a silicon wafer etched by a method according to any one of claims 1 to 6, and differentiating a surface and rear surface of a wafer. By carrying out mirror polishing only of the wafer surface which obtained good display flatness by etching, and made rear-face granularity small in an invention concerning claim 7, It has display flatness with highly precise wafer both sides, and small surface roughness, and a wafer surface has a degree of brilliancy for which a device maker asks, and a surface and rear surface of a wafer becomes identifiable by viewing.

[0009]

[Embodiment of the Invention]Next, an embodiment of the invention is described based on a drawing. The etching method of the silicon wafer concerning this invention, Acid etching liquid and alkali etching liquid are stored in two or more etching tubs, respectively, Are the silicon wafer which has the damaged layer which passed through the washing process following the lapping process improvement of the method of immersing in acid etching liquid and alkali etching liquid one by one, and this characteristic composition, It is in the place carried out in 0.2micrometers/[a second and] or more in the sum total with which alkali etching made concentration of a line crack and alkali etching liquid 8 or more mol/l after acid etching, and the surface and the rear face of the silicon wafer were doubled for the etching rate of acid etching.

[0010]. The shape of the facet formed in a wafer as the concentration of alkali etching liquid is less than a lower limit becomes large. A size needs to enlarge the polish cost of the chemical and mechanical grinding which surface roughness produces the fault which becomes large and performs by a post process which a 10 to about tens of microns deep pit generates in several microns or less in the depth. As for the concentration of alkali etching liquid, 10 or more mol/l is preferred. As for the etching rate of acid etching, a second is preferred in 0.2-0.8micrometer /.

[0011]The degree of brilliancy is defined by JIS (JIS Z 8741) here. According to this standard, a degree of brilliancy is expressed to a certain sample face as a numerical value as which the refractive index of specular light bunch psis of the light which entered by the incidence angle theta displayed the rate over specular light bunch $psis_0$ in the same system of measurement of the glass surface of 1.567 at percent. The incidence angle theta in the case of the formula showing in a following formula (1) being able to express the degree of brilliancy Gr (theta), and measuring the degree of brilliancy of a silicon wafer surface is 60 degrees.

[0012]

[Equation 1]

$$\text{光沢度 } Gr(\theta) = \frac{\Psi_S}{\Psi_{S_0}} \times 100 \qquad \cdots\cdots (1)$$

[0013]The etching mechanism of acid etching was included in nitric acid etc., or consists of oxidation of the silicon by the oxidation seed included in another compound, and removal of the oxide with another reducing compounds, such as fluoric acid. In order to control the etching rate of this acid etching,

acetic acid, sulfuric acid, phosphoric acid, water, etc. are added as a diluent. The addition solution used for these diluents has another effect of changing the surface tension and viscosity of acid etching liquid, and is properly used by the purpose. The etching rate of acid etching liquid falls by generally adding a diluent. It is in the tendency for surface granularity to become large, with the fall of an etching rate. Therefore, the effect that Ra which is an index of surface roughness becomes large and that a degree of brilliancy becomes small shows up. From the reason of the homogeneity within a wafer surface improving about the heat generated in connection with an etching reaction, display flatness shows the tendency which becomes good as an etching rate becomes small.

[0014]A wafer is etched so that the sum total with which, as for a sum total machining allowance of 13-25 micrometers and an alkali etching tub, the sum total with which a sum total machining allowance of an acid etching tub doubled the surface and a rear face of a silicon wafer doubled the surface and a rear face of a silicon wafer may be set to 5-13 micrometers. If fault in which a machining allowance is [that surface roughness becomes it large that a sum total machining allowance of acid etching is less than a lower limit] correctly uncontrollable is produced and upper limit is exceeded, a wave of several millimeter order called nano topography will produce fault which becomes large. If it does not become a numerical value of a request of a degree of brilliancy by a sum total machining allowance of alkali etching being less than a lower limit but upper limit is exceeded, fault which nano topography generates will be produced. A sum total machining allowance of 13-20 micrometers and an alkali etching tub has [5-10 micrometers] a preferred sum total machining allowance of an acid etching tub.

[0015]The number of etching tubs of this invention is two to 6 tub. Combination of an acid etching tub and an alkali etching tub is shown in Table 1.

[0016]

[Table 1]

エッチング槽の数	酸エッチング槽とアルカリエッチング槽との組合せ
2槽	酸－アルカリ
3槽	酸－酸－アルカリ 酸－アルカリ－酸 酸－アルカリ－アルカリ
4槽	酸－酸－酸－アルカリ 酸－酸－アルカリ－酸 酸－酸－アルカリ－アルカリ 酸－アルカリ－酸－酸 酸－アルカリ－酸－アルカリ 酸－アルカリ－アルカリ－酸 酸－アルカリ－アルカリ－アルカリ
5槽	酸－酸－酸－アルカリ－アルカリ 酸－酸－アルカリ－酸－アルカリ 酸－酸－アルカリ－アルカリ－酸 酸－酸－アルカリ－アルカリ－アルカリ 酸－アルカリ－酸－酸－アルカリ 酸－アルカリ－酸－アルカリ－酸 酸－アルカリ－酸－アルカリ－アルカリ 酸－アルカリ－アルカリ－酸－酸 酸－アルカリ－アルカリ－酸－アルカリ 酸－アルカリ－アルカリ－アルカリ－酸
6槽	酸－酸－酸－アルカリ－アルカリ－アルカリ 酸－酸－アルカリ－酸－アルカリ－アルカリ 酸－酸－アルカリ－アルカリ－酸－アルカリ 酸－酸－アルカリ－アルカリ－アルカリ－酸 酸－アルカリ－酸－酸－アルカリ－アルカリ 酸－アルカリ－酸－アルカリ－酸－アルカリ 酸－アルカリ－酸－アルカリ－アルカリ－酸 酸－アルカリ－アルカリ－酸－酸－アルカリ 酸－アルカリ－アルカリ－酸－アルカリ－酸 酸－アルカリ－アルカリ－アルカリ－酸－酸

[0017]If the number of etching tubs exceeds upper limit, surface roughness of a wafer will get worse. The number of desirable etching tubs is two to 3 tub, and an acid etching tub is [one tub and an alkali etching tub of the optimal mode in this case] two or less tubs. For example, when the number of etching tubs is two tubs, a wafer is immersed in order of an acid etching tub and an alkali etching tub. When the number of etching tubs is three tubs, a wafer will be immersed in order of an acid etching tub, an alkali etching tub, and an alkali etching tub.

[0018]Between an acid etching process and an acid etching process, although it is not necessary to carry out between an alkali etching process and an alkali etching process by performing the rinse processes immersed in a rinse tub, between an acid etching process and an alkali etching process, rinse processes are certainly performed. Since the acid which adhered to the wafer by putting in these rinse

processes in between is washed out, a possibility of causing the alkali and the reaction in a next process disappears. As for acid etching liquid, it is preferred that fluoric acid and nitric acid are included, respectively, and acetic acid, sulfuric acid, or at least one sort of phosphoric acid is included further. The liquid in which alkali etching liquid contains sodium hydroxide or a potassium hydrate is used.

[0019]Since a wafer surface has a degree of brilliancy higher than a wafer rear face, the wafer obtained by carrying out mirror polishing only of the surface of the silicon wafer etched by the etching method of this invention can differentiate a surface and rear surface to an identifiable grade.

[0020]

[Example]Next, the example of this invention is described in detail with a comparative example. <Example 1> The silicon wafer which has the damaged layer which passed through the washing process following the lapping process first was prepared. Subsequently, the acid etching liquid which will mix acetic acid 90wt% and water and in which an etching rate will be a second in 0.5micrometer /was prepared nitric acid 70wt% fluoric acid 50wt%. Concentration prepared the alkali etching liquid which uses the potassium hydrate of 8.5 mol/l as the main ingredients. The prepared acid etching liquid was stored in the etching tub of one tub, solution temperature was maintained at 30 **, similarly, alkali etching liquid was stored in the etching tub of one tub, and solution temperature was maintained at 80 **. Subsequently, it etched by following 15 micrometers as a rule of thumb, and being immersed for 30 seconds in the sum total which immersed the above-mentioned wafer and with which the surface and the rear face of the silicon wafer were doubled for the machining allowance of the wafer, agitating the etching reagent in an acid etching tub. It rinsed by immersing the wafer which finished acid etching in ultrapure water. Next, it etched by following 10 micrometers as a rule of thumb, and being immersed for 240 seconds in the sum total which immersed the wafer which finished the above-mentioned rinse and with which the surface and the rear face of the silicon wafer were doubled for the machining allowance of the wafer, agitating the etching reagent in an alkali etching tub. It dried, after immersing the wafer which finished alkali etching in ultrapure water and rinsing it.

[0021]The etching process of the wafer was carried out like Example 1 except having carried out to acetic acid 90wt%, and having made the etching rate of acid into a second in 0.3micrometer /nitric acid 70wt%, <Example 2> fluoric acid 50wt%.

[0022]The etching process of the wafer was carried out like Example 1 except having carried out to acetic acid 90wt%, and having made the etching rate of acid into a second in 0.1micrometer /nitric acid 70wt%, <comparative example 1> fluoric acid 50wt%.

[0023]The surface roughness on the rear face of a wafer which finished the etching process of the <comparative study> examples 1 and 2 and the comparative example 1, and a degree of brilliancy were measured, respectively. Surface roughness is measured with an optical surface roughness measuring instrument (product made from chapman), The degree of brilliancy was measured based on JIS (JISZ 8741) using the glossmeter (made by Nippon Denshoku Co., Ltd.), and made what was made into the percentage of the value which **(ed) the numerical value acquired further at 360% which is a numerical value of the surface degree of brilliancy after mirror polishing the rear-face degree of brilliancy when the surface degree of brilliancy was made into 100%. A measurement result is shown in Table 2, respectively.

[0024]

[Table 2]

	酸エッチング レート (μm/秒)	アルカリエッチング 濃度 (mol/l)	表面粗さRa (Å)	光沢度(%)
実施例 1	0.5	8.5	2076	53.3
〃 2	0.3	8.5	2785	44.6
比較例 1	0.1	8.5	3399	37.8

[0025]the numerical value of granularity Ra on the rear face of a wafer which passed through the etching process in Examples 1 and 2 with a large etching rate of acid to the comparative example 1 with a small etching rate of acid becomes small so that more clearly than Table 2 -- a degree of brilliancy -- a rear surface -- it turns out that it is an identifiable range.

[0026]

[Effect of the Invention]As stated above, according to this invention, acid etching liquid and alkali etching liquid are stored in two or more etching tubs, respectively, It is improvement of the etching method of the silicon wafer which immerses the silicon wafer which has the damaged layer which passed through the washing process following the lapping process one by one in acid etching liquid and alkali etching liquid. It is in the place carried out in 0.2micrometers/[a second and] or more in the sum total with which alkali etching made concentration of a line crack and alkali etching liquid 8 or more mol/l after acid etching, and the surface and the rear face of the silicon wafer were doubled for the etching rate of acid etching. By specifying acid and alkali etching on the above-mentioned conditions, the rear-face display flatness, the degree of brilliancy, and surface roughness for which a device maker asks are obtained.

[0027]For this reason, by giving mirror polishing which is a post process only to the surface of the wafer obtained by this etching, In a wafer surface, a degree of brilliancy becomes high from a wafer rear face, and wafer both sides have highly precise display flatness and small surface roughness, Problems in detection of the wafer existence in the conveyance system of a device process, such as detection difficulty and wrong detection, are not produced, but the surface and rear surface of a wafer can be differentiated to an identifiable grade by viewing.

[Translation done.]